adjusting the phase of a clock signal based on the stored offset value to produce a phase adjusted clock signal; and

transmitting data over the data line based on the phase adjusted clock signal.

23. The method of claim 22, wherein transmitting data over the data line further comprises driving the data on the data line using an output buffer, wherein timing of the output buffer is controlled based on the phase adjusted clock signal.

24. The method of claim 21, wherein determining the phase offset value further comprises sending data to the first slave device.

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25. The method of claim 24, wherein the data is sent to the first slave device over a request line.

26. The method of claim 24, wherein determining the phase offset value further comprises receiving the data sent to the first slave device, from the first slave device.

27. The method of claim 26, wherein determining the phase offset value further comprises comparing phase of the data received from the first slave device with phase of a clock signal.

28. The method of claim 27, wherein the data is sent to the first slave device over a request line, and wherein the data is received from the first slave device over the data line.

29. The method of claim 21, wherein the phase offset value is stored with a plurality of additional phase offset values in the master device.

30. The method of claim 21, wherein the phase offset value is adjusted by a margin offset.

31. The method of claim 21 further comprises:

determining a control phase offset value corresponding to control information transmission from the master device to a second slave device over a request line;

storing the control phase offset value in the master device to produce a stored control offset value; and

using the stored control offset value in the transmission of control information from the master device to the second slave device over the request line.

32. The method of claim 31, wherein using the stored control offset value further comprises:

adjusting the phase of a clock signal based on the stored control offset value to produce a phase adjusted clock signal; and

transmitting control information over the request line based on the phase adjusted clock signal.

33. The method of claim 32, wherein transmitting control information over the request line further comprises driving the control information on the request line using an output buffer, wherein the timing of the output buffer is controlled based on the phase adjusted clock signal.

34. The method of claim 31, wherein the control information includes a slave access request.

35. The method of claim 21, wherein using the stored offset value further comprises using the stored offset value in the transmission of data over a plurality of data lines.

36. The method of claim 35, wherein using the stored offset value further comprises:

adjusting the phase of a clock signal based on the stored offset value to produce a phase adjusted clock signal; and

driving data on the plurality of data lines using a corresponding plurality of output buffers, wherein timing of each output buffer of the plurality of output buffers is controlled based on the stored offset value.

37. A method for calibrating transmission of control information from a master device to a first slave device over a request line, comprising:

determining a phase offset value corresponding to control information transmission from the master device to the first slave device over the request line;

storing the phase offset value in the master device to produce a stored offset value;

retrieving the stored offset value; and

using the stored offset value in the transmission of control information from the master device to the first slave device over the request line.

38. The method of claim 37, wherein using the stored offset value further comprises:

adjusting the phase of a clock signal based on the stored offset value to produce a phase adjusted clock signal; and

transmitting control information over the request line based on the phase adjusted clock signal.

39. The method of claim 38, wherein transmitting control information over the request line further comprises driving the control information on the data line using an output buffer, wherein timing of the output buffer is controlled based on the phase adjusted clock signal.

40. The method of claim 37, wherein determining the phase offset value further comprises sending data to the first slave device.

41. The method of claim 40, wherein sending data to the first slave device further comprises sending data to the first slave device over the request line.

42. The method of claim 40, wherein determining the phase offset value further comprises receiving the data sent to the first slave device, from the first slave device.

43. The method of claim 42, wherein determining the phase offset value further comprises comparing phase of the data received from the first slave device with phase of a clock signal.

44. The method of claim 43, wherein the data is sent to the first slave device over the request line, and wherein the data is received from the first slave device over a data line.

45. The method of claim 37, wherein the phase offset value is stored with a plurality of additional phase offset values in the master device.

46. The method of claim 37, wherein the phase offset value is adjusted by a margin offset.

47. The method of claim 37, wherein using the stored offset value further comprises using the stored offset value in the transmission of control information over a plurality of request lines.

48. The method of claim 47, wherein using the stored offset value further comprises:

adjusting the phase of a clock signal based on the stored offset value to produce a phase adjusted clock signal; and

driving control information on the plurality of request lines using a corresponding plurality of output buffers, wherein timing of each output buffer of the plurality of output buffers is controlled based on the stored offset value.

49. The method of claim 37, wherein the control information transmitted to the slave device is a portion of an access request.

50. A master device operable to transmit data to a first slave device over a data line, the master device comprising:

a phase aligner operable to determine a phase offset value corresponding to data transmission from the master device to the first slave device over the data line, wherein the

phase aligner includes a first register operable to store the phase offset value as a stored offset; and

an output buffer operably coupled to the phase aligner, wherein the output buffer is operable to drive the data on the data line based on the stored offset.

51. The master device of claim 50, wherein the phase aligner includes a phase rotator operable to receive a clock signal, wherein the phase rotator is operable to generate a phase adjusted clock signal from the clock signal based on the stored offset, wherein timing of the output buffer is controlled based on the phase adjusted clock signal.

52. The master device of claim 51, wherein the phase rotator includes a phase locked loop.

53. The master device of claim 51, wherein the phase rotator includes a delay locked loop.

54. The master device of claim 50, wherein the phase aligner periodically determines the phase offset value corresponding to data transmission and stores the periodically determined phase offset value in the first register.

55. The master device of claim 50, wherein the phase offset value is at least partially based on flight time of the data on the data line.

56. The master device of claim 50 further comprising a logic block operable to generate data that is sent to the first slave device in order to determine the phase offset value.

57. The master device of claim 50 further comprising receiving circuitry operable to receive data from the first slave device, wherein the data received from the first slave device is used by the phase aligner to determine the phase offset value.

58. The master device of claim 57, wherein the phase aligner is operable to compare the data received from the first slave device with a clock signal to determine the phase offset value.

59. The master device of claim 50 further comprising a plurality of output drivers coupled to the phase aligner, wherein each output driver of the plurality of output drivers drives data onto a corresponding data line based on the stored offset.

60. The master device of claim 50, wherein the phase aligner is operable to determine a control phase offset value corresponding to control information transmission from the master device to a second slave device over a request line, wherein the phase aligner includes a second register operable to store the control phase offset value as a stored control offset.

61. The master device of claim 60 further comprising a control output driver operably coupled to the phase aligner, wherein the control output driver is operable to drive control information on the request line based on the stored control offset.

62. The master device of claim 61, wherein the phase aligner includes a phase rotator operable to receive a clock signal, wherein the phase rotator is operable to generate a phase adjusted clock signal from the clock signal based on the control phase offset, wherein timing of the control output driver is controlled based on the phase adjusted clock signal.

63. The master device of claim 60 further comprising a plurality of control output drivers operably coupled to the phase aligner, wherein each control output driver of the plurality of control output drivers is operable to drive control information on a corresponding request line based on the stored control offset.

64. A master device operable to transmit control information to a first slave device over a request line, the master device comprising:

a phase aligner operable to determine a phase offset value corresponding to control information transmission from the master device to the first slave device over the request line, wherein the phase aligner includes a register operable to store the phase offset value as a stored offset; and

an output buffer operably coupled to the phase aligner, wherein the output buffer is operable to drive the control information on the request line based on the stored offset.

65. The master device of claim 64, wherein the phase aligner includes a phase rotator operable to receive a clock signal, wherein the phase aligner is operable to generate a phase adjusted clock signal from the clock signal based on the stored offset, wherein timing of the output buffer is controlled based on the phase adjusted clock signal.

66. The master device of claim 65, wherein the phase rotator includes a phase locked loop.

67. The master device of claim 65, wherein the phase rotator includes a delay locked loop.

68. The master device of claim 64, wherein the phase aligner periodically determines the phase offset value corresponding to data transmission and stores the periodically determined phase offset value in the first register.

69. The master device of claim 64, wherein the phase offset value is at least partially based on flight time of the control information on the request line.

70. The master device of claim 74 further comprising a logic block operable to generate data that is sent to the first slave device in order to determine the phase offset value.

71. The master device of claim 64 further comprising receiving circuitry operable to receive data from the first slave device, wherein the data received from the first slave device is used by the phase aligner to determine the phase offset value.

72. The master device of claim 71, wherein the phase aligner is operable to compare the data received from the first slave device with a clock signal to determine the phase offset value.

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73. The master device of claim 64 further comprising a plurality of output drivers coupled to the phase aligner, wherein each output driver of the plurality of output drivers outputs drives control information onto a corresponding request line based on the stored offset.